REMARKS

This is a full and timely response to the Office Action mailed May 25, 2010. Claims 1-16 have been cancelled. New claims 17-36 have been added. *These amendments add no new matter.* Support for these amendments may be found variously throughout the Specification, including, but not limited to page 9, line 16 to page 15, line 9 of the Substitute Specification and FIGS. 4 and 5.

Reexamination in light of the following remarks is respectfully requested.

I. Rejections under 35 U.S.C. §112

Claims 1, 3, 4, 5, 7, 8, and 10-16 have been rejected under 35 U.S.C. §112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter that applicant regards as the invention.

In view of the cancellation of claims 1, 3, 4, 5, 7, 8, and 10-16, Applicants submit that the rejection of these claims is now moot and requests that the rejection of these claims be withdrawn.

II. Rejections under 35 U.S.C. §103

Claims 1, 3, 4, 5, 7, 8, and 10-16 (and withdrawn claims 6 and 9) have been rejected under 35 U.S.C. § 103(a) as being unpatentable over EP 1 014 334 A2 to Nakajima et al. ("Nakajima") in view of U.S. Pub. No. 2003/0011584 A1 to Azami et al. ("Azami").

In view of the cancellation of claims 1, 3, 4, 5, 7, 8, and 10-16 (and withdrawn claims 6 and 9), Applicants submit that the rejection of these claims is now moot and requests that the rejection of these claims be withdrawn.

III. New Claims 17-36

New claims 17-36 have been added. Claims 18-36 depend from generic, independent claim 17. These claims are believed to be in condition for allowance.

New claim 17 recites: *[a] data transfer circuit comprising:*

a first latch section that outputs a single-phase first latch result; and

a second latch section that latches said single-phase first latch result,

wherein said first latch section includes a first inverter and a second inverter, an input from said first inverter being inputted to said second inverter via a switching circuit, and

wherein a power supply voltage of said first latch section is raised from a first voltage to a second voltage while said single-phase first latch result is transferred to said second latch section.

In order to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974); *see also* MPEP 2143.03.

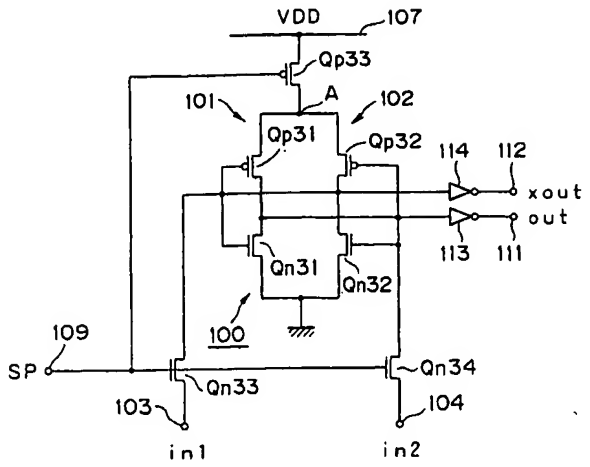
Nakajima and Azami, either alone or in any permissible combination, fail to disclose or suggest these features. Specifically, Nakajima and Azami, fail to disclose or suggest "*wherein said first latch section includes a first inverter and a second inverter, an input from said first inverter being inputted to said second inverter via a switching circuit.*"

Nakajima discloses a drive circuit having a first and second latch. (Nakajima, FIGS. 1, 21, and 23; paras. [0105]-[0107]).

The Office Action asserts that Nakajima discloses "an output from said first inverter [*e.g., Fig. 21: 101*] is inputted to said second inverter [*e.g., Fig. 21: 102*] via a switching circuit [*e.g., Fig. 21: Qp33*] that operates off-action at a sampling pulse [*e.g., Fig. 21: SP*]." (Office Action, p. 26, ll. 5-8). But this is not the case.

As shown in Nakajima Fig. 21, reproduced below, Nakajima discloses "the PMOS transistor Qp33 is utilized as the power supply side switch 108, and a sampling pulse SP is directly applied to the gates of [this] transistor[]." (Nakajima, para. [0189]).

FIG. 21



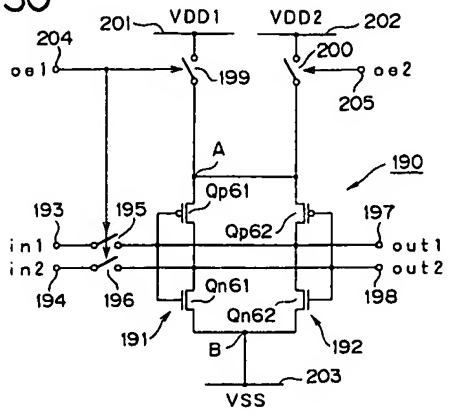
Nakajima - Fig. 21

Thus, while Nakajima discloses a PMOS transistor Qp33 as a power supply switch for CMOS inverters 101 and 102, it is *NOT* the case that Nakajima discloses "*wherein said first latch section includes a first inverter and a second inverter, an input from said first inverter being inputted to said second inverter via a switching circuit.*"

The Office Action further asserts that Nakajima discloses "an output from said first inverter [*e.g., Fig. 30: 191; Fig. 31: 211*] is inputted to said second inverter [*e.g., Fig. 30: 192; Fig. 31: 212*] via a switching circuit [*e.g., Fig. 30: 200; Fig. 31: 220*] that operates off-action at a sampling pulse [*e.g., Fig. 30: oe2; Fig. 31: oe2*]." (Office Action, p. 26, ll. 12-15). But again, this is not the case.

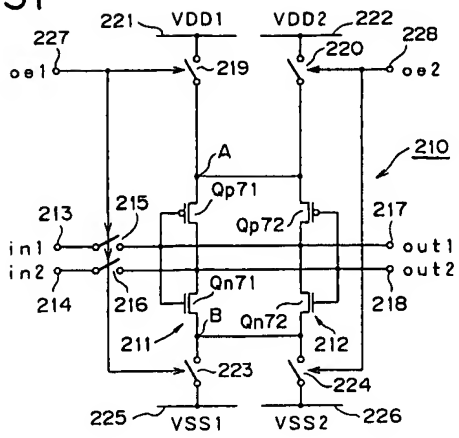
As shown in Nakajima Figs. 30 and 31, reproduced below-left and below right, respectively, Nakajima discloses "node A is also connected by way of the switch 200 to the power supply line 202 ... controlled by an output enable pulse oe2." (Nakajima, paras. [0229] and [0230]), and "node A is also connected by way of the switch 220 to the power supply line 222 ... [t]he switching of the switch[] 220 ... [being] controlled by an output enable pulse oe2." (Nakajima, paras. [0238] and [0239]).

FIG. 30



Nakajima - Fig. 30

FIG. 31



Nakajima - Fig. 31

Thus, while Nakajima discloses switches 200 and 220 as a power supply switches for CMOS inverters 191 and 192, and 211 and 212, it is *NOT* the case that Nakajima discloses "*wherein said first latch section includes a first inverter and a second inverter, an input from said first inverter being inputted to said second inverter via a switching circuit.*"

Azami is relied upon in the Office Action, but Azami fails to remedy the deficiencies of Nakajima. Azami discloses a first latch circuit and a second latch circuit used in a light emitting device. (Azami, FIG. 18; *see also* Azami, para. [0183]).

But Azami, like Nakajima, fails to disclose "*wherein said first latch section includes a first inverter and a second inverter, an input from said first inverter being inputted to said second inverter via a switching circuit.*"

Because Nakajima and Azami, either alone or in any permissible combination, fail to disclose or suggest all the features recited by claim 17, claim 17is believed to be in condition for allowance.

Claims 18-36, which depend from claim 17, are distinct for their incorporation of the features recited by claim 17, as well as their separately recited patentably distinct features. Thus, claims 18-36 are also believed to be in condition for allowance.

IV. Conclusion

In view of the above amendment and remarks, applicant believes the pending application is in condition for allowance.

This response is believed to be a complete response to the Office Action. However, Applicant reserves the right to set forth further arguments supporting the patentability of the claims, including the separate patentability of the dependent claims not explicitly addressed herein, in future papers. Further, for any instances in which the Examiner took Official Notice in the Office Action, Applicant expressly does not acquiesce to the taking of Official Notice, and respectfully requests that the Examiner provide an affidavit to support the Official Notice taken in the next Office Action, as required by 37 CFR 1.104(d)(2) and MPEP § 2144.03.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 18-0013, under Order No. SON-3055 from which the undersigned is authorized to draw.

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Respectfully submitted,

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